TDA3566A
PAL/NTSC decoder

Product specification
Supersedes data of March 1991
File under Integrated Circuits, IC02

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Philips Semiconductors

FEATURES

- A black-current stabilizer which controls the black-currents of the three electron-guns to a level low enough to omit the black-level adjustment
- Contrast control of inserted RGB signals
- No black-level disturbance when non-synchronized external RGB signals are available on the inputs
- NTSC capability with hue control.

APPLICATIONS

- Teletext/broadcast antiope
- Channel number display.

GENERAL DESCRIPTION

The TDA3566A is a decoder for the PAL and/or NTSC colour television standards. It combines all functions required for the identification and demodulation of PAL/NTSC signals.

Furthermore it contains a luminance amplifier, an RGB-matrix and amplifier. These amplifiers supply output signals up to 4 V peak-to-peak (picture information) enabling direct drive of the discrete output stages. The circuit also contains separate inputs for data insertion, analog and digital, which can be used for text display systems.

QUICK REFERENCE DATA

All voltages referenced to ground.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Supply					
V_P	supply voltage (pin 1)	–	12	–	V
I_P	supply current (pin 1)	–	90	–	mA
Luminance amplifier (pin 8)					
$V_{8(p-p)}$	input voltage (peak-to-peak value)	–	450	–	mV
CON	contrast control	–	16.5	–	dB
Chrominance amplifier (pin 4)					
$V_{4(p-p)}$	input voltage (peak-to-peak value)	40	–	1100	mV
SAT	saturation control	–	50	–	dB
RGB matrix and amplifiers					
$V_{13,\ 15,\ 17(p-p)}$	output voltage at nominal luminance and contrast (peak-to-peak value)	–	3.8	–	V
Data insertion					
$V_{12,\ 14,\ 16(p-p)}$	input signals (peak-to-peak value)	–	1	–	V
Data blanking (pin 9)					
V_9	input voltage for data insertion	0.9	–	–	V
Sandcastle input (pin 7)					
V_7	blanking input voltage	–	1.5	–	V
V_7	burst gating and clamping input voltage	–	7	–	V

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA3566A	28	DIL	plastic	SOT117

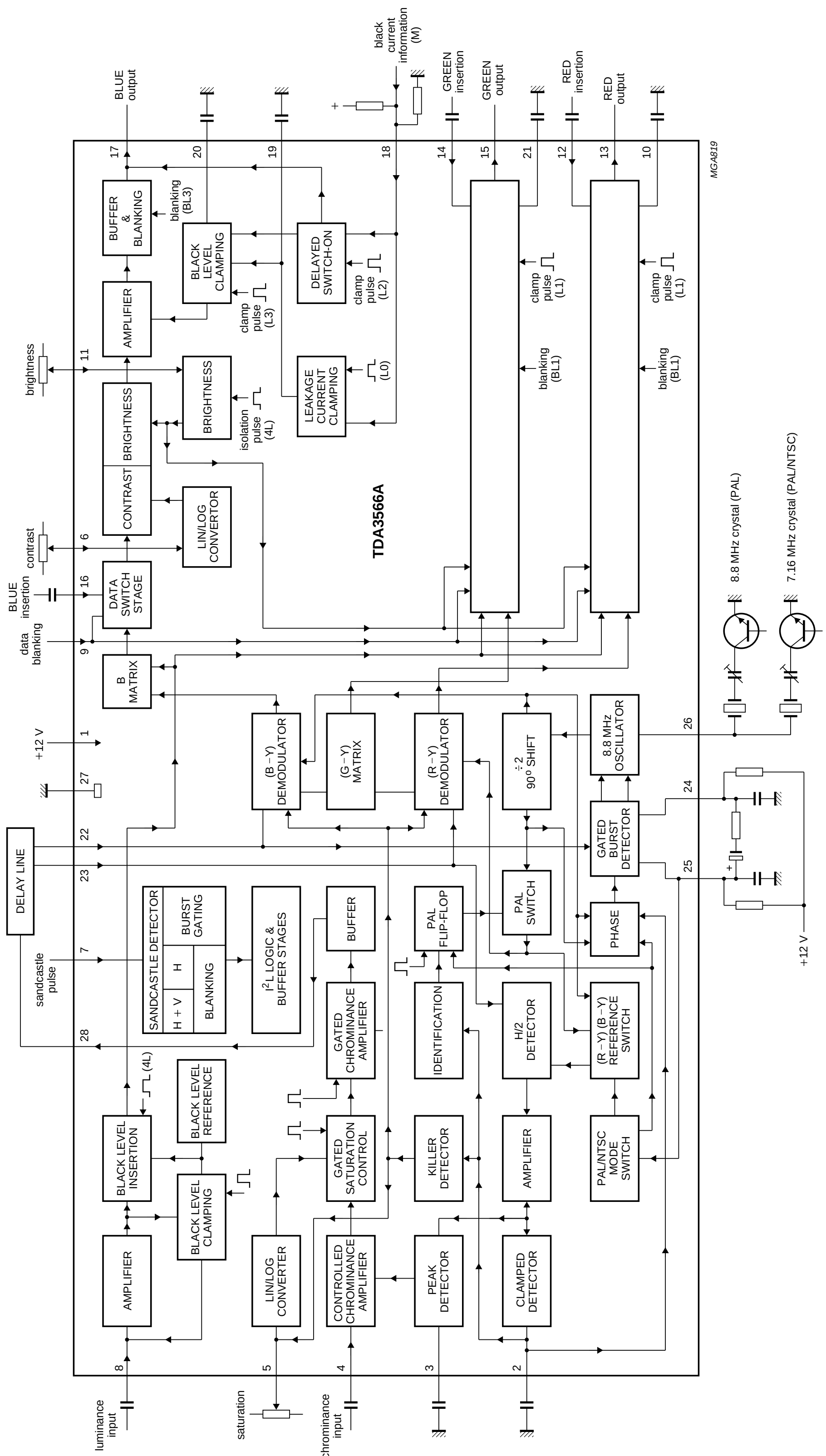


Fig.1 Block diagram.

For explanation of pulse mnemonics see Fig. 7.

PINNING

SYMBOL	PIN	DESCRIPTION
V_P	1	supply voltage
IDDET	2	identification detection level
ACCDET	3	Automatic Chrominance Control detection level
CHR_{IN}	4	chrominance control input
SAT	5	saturation control input
CON	6	contrast control input
SC	7	sandcastle input
LUM	8	luminance control input
DBL	9	data blanking input
BCL_R	10	black clamp level for RED output
BRI	11	brightness input
R_{IN}	12	RED input
R_{OUT}	13	RED output
G_{IN}	14	GREEN input
G_{OUT}	15	GREEN output
B_{IN}	16	BLUE input
B_{OUT}	17	BLUE output
BLA	18	black current input
BCL	19	black clamp level; referenced to black level
BCL_B	20	black clamp level for BLUE output
BCL_G	21	black clamp level for GREEN output
B–Y	22	demodulator input (BLUE)
R–Y	23	demodulator input (RED)
RCEXT	24	gated burst detector load network
RCEXT	25	gated burst detector load network
OSC	26	oscillator frequency input
GND	27	ground
CHR_{OUT}	28	chrominance signal output

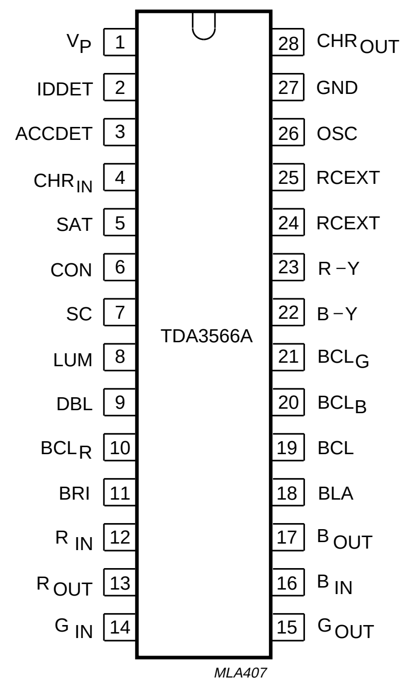


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA3566A is a further development of the TDA3562A. It has the same pinning and nearly the same application. The differences between the TDA3562A and the TDA3566A are as follows:

- The NTSC-application has largely been simplified. In the event of NTSC the chrominance signal is now internally coupled to the demodulators, automatic chrominance control (ACC) and phase detectors. The chrominance output signal (pin 28) is thus suppressed. It follows that the external switches and filters which are required for the TDA3562A are not required for the TDA3566A. There is no difference between the amplitudes of the colour output signals in the PAL or NTSC mode.
- The clamp capacitor at pins 10, 20 and 21 in the black-level stabilization loop can be reduced to 100 nF provided the stability of the loop is maintained. Loop stability depends on complete application. The clamp capacitors receive a pre-bias voltage to avoid coloured background during switch-on.
- The crystal oscillator circuit has been changed to prevent parasitic oscillations on the third overtone of the crystal. Consequently the optimum tuning capacitance must be reduced to 10 pF.
- The hue control has been improved (linear).

Luminance amplifier

The luminance amplifier is voltage driven and requires an input signal of 450 mV peak-to-peak (positive video). The luminance delay line must be connected between the IF amplifier and the decoder.

The input signal is AC coupled to the input (pin 8). After amplification, the black level at the output of the preamplifier is clamped to a fixed DC level by the black level clamping circuit. During three line periods after vertical blanking, the luminance signal is blanked out and the black level reference voltage is inserted by a switching circuit.

This black level reference voltage is controlled via pin11 (brightness). At the same time the RGB signals are clamped. Noise and residual signals have no influence during clamping thus simple internal clamping circuitry is used.

Chrominance amplifiers

The chrominance amplifier has an asymmetrical input. The input signal must be AC coupled (pin 4) and have a minimum amplitude of 40 mV peak-to-peak.

The gain control stage has a control range in excess of 30 dB, the maximum input signal must not exceed 1.1 V peak-to-peak, otherwise clipping of the input signal will occur.

From the gain control stage the chrominance signal is fed to the saturation control stage. Saturation is linearly controlled via pin 5. The control voltage range is 2 to 4 V, the input impedance is high and the saturation control range is in excess of 50 dB.

The burst signal is not affected by saturation control. The signal is then fed to a gated amplifier which has a 12 dB higher gain during the chrominance signal. As a result the signal at the output (pin 28) has a burst-to-chrominance ratio which is 6 dB lower than that of the input signal when the saturation control is set at –6 dB.

The chrominance output signal is fed to the delay line and, after matrixing, is applied to the demodulator input pins (pins 22 and 23). These signals are fed to the burst phase detector. In the event of NTSC the chrominance signal is internally coupled to the demodulators, ACC and phase detectors.

Oscillator and identification circuit

The burst phase detector is gated with the narrow part of the sandcastle pulse (pin 7). In the detector the (R–Y) and (B–Y) signals are added to provide the composite burst signal again.

This composite signal is compared with the oscillator signal divided-by-2 (R–Y) reference signal. The control voltage is available at pins 24 and 25, and is also applied to the 8.8 MHz oscillator. The 4.4 MHz signal is obtained via the divide-by-2 circuit, which generates both the (B–Y) and (R–Y) reference signals and provides a 90° phase shift between them.

The flip-flop is driven by pulses obtained from the sandcastle detector. For the identification of the phase at PAL mode, the (R–Y) reference signal coming from the PAL switch, is compared to the vertical signal (R–Y) of the PAL delay line. This is carried out in the H/2 detector, which is gated during burst.

When the phase is incorrect, the flip-flop gets a reset from the identification circuit. When the phase is correct, the output voltage of the H/2 detector is directly related to the burst amplitude so that this voltage can be used for the ACC.

To avoid 'blooming-up' of the picture under weak input signal conditions the ACC voltage is generated by peak detection of the H/2 detector output signal. The killer and identification circuits receive their information from a gated output signal of H/2 detector. Killing is obtained via the saturation control stage and the demodulators to obtain good suppression.

The time constant of the saturation control (pin 5) provides a delayed switch-on after killing. Adjustment of the oscillator is achieved by variation of the burst phase detector load resistance between pins 24 and 25 (see Fig.8).

With this application the trimmer capacitor in series with the 8.8 MHz crystal (pin 26) can be replaced by a fixed value capacitor to compensate for unbalance of the phase detector.

Demodulator

The (R–Y) and (B–Y) demodulators are driven by the colour difference signals from the delay-line matrix circuit and the reference signals from the 8.8 MHz divider circuit. The (R–Y) reference signal is fed via the PAL-switch. The output signals are fed to the R and B matrix circuits and to the (G–Y) matrix to provide the (G–Y) signal which is applied to the G-matrix. The demodulation circuits are killed and blanked by by-passing the input signals.

NTSC mode

The NTSC mode is switched on when the voltage at the burst phase detector outputs (pins 24 and 25) is adjusted below 9 V.

To ensure reliable application the phase detector load resistors are external. When the TDA3566A is used only for PAL these two 33 kΩ resistors must be connected to +12 V (see Fig.8).

For PAL/NTSC application the value of each resistor must be reduced to 20 kΩ (with a tolerance of 1%) and connected to the slider of a potentiometer (see Fig.9). The switching transistor brings the voltage at pins 24 and 25 below 9 V which switches the circuit tot the NTSC mode.

The position of the PAL flip-flop ensures that the correct phase of the (R–Y) reference signal is supplied to the (R–Y) demodulator.

The drive to the H/2 detector is now provided by the (B–Y) reference signal. In the PAL mode it is driven by the (R–Y) reference signal. Hue control is realized by changing the phase of the reference drive to the burst phase detector.

This is achieved by varying the voltage at pins 24 and 25 between 7.0 V and 8.5 V, nominal position 7.65 V. The hue control characteristic is shown in Fig.6.

RGB matrix and amplifiers

The three matrix and amplifier circuits are identical and only one circuit will be described.

The luminance and the colour difference signals are added in the matrix circuit to obtain the colour signal, which is then fed to the contrast control stage.

The contrast control voltage is supplied to pin 6 (high-input impedance). The control range is +5 dB to –11.5 dB nominal. The relationship between the control voltage and the gain is linear (see Fig.3).

During the 3-line period after blanking a pulse is inserted at the output of the contrast control stage. The amplitude of this pulse is varied by a control voltage at pin 11. This applies a variable offset to the normal black level, thus providing brightness control.

The brightness control range is 1 V to 3.6 V. While this offset level is present, the black-current input impedance (pin 18) is high and the internal clamp circuit is activated. The clamp circuit then compares the reference voltage at pin 19 with the voltage developed across the external resistor network R_A and R_B (pin 18) which is provided by picture tube beam current.

The output of the comparator is stored in capacitors connected from pins 10, 20 and 21 to ground which controls the black level at the output.

The reference voltage is composed by the resistor divider network and the leakage current of the picture tube into this bleeder. During vertical blanking, this voltage is stored in the capacitor connected to pin 19, which ensures that the leakage current of the CRT does not influence the black current measurement.

The RGB output signals can never exceed a level of 10.6 V. When the signal tends to exceed this level the output signal is clipped. The black level at the outputs (pins 13, 15 and 17) will be approximately 3 V. This level depends on the spread of the guns of the picture tube. If a beam current stabilizer is not used it is possible to stabilize the black levels at the outputs, which in this application must be connected to the black current measuring input (pin 18) via a resistor network.

Data insertion

Each colour amplifier has a separate input for data insertion.
A 1 V peak-to-peak input signal provides a 3.8 V peak-to-peak output signal.

To avoid the black-level of the inserted signal differing from the black level of the normal video signal, the data is clamped to the black level of the luminance signal. Therefore AC coupling is required for the data inputs.

To avoid a disturbance of the blanking level due to the clamping circuit, the source impedance of the driver circuit must not exceed 150 Ω. The data insertion circuit is activated by the data blanking input (pin 9). When the voltage at this pin exceeds a level of 0.9 V, the RGB matrix circuits are switched off and the data amplifiers are switched on.

To avoid coloured edges, the data blanking switching time is short. The amplitude of the data output signals is controlled by the contrast control at pin 6. The black level is equal to the video black level and can be varied between 2 and 4 V (nominal condition) by the brightness control voltage at pin 11.

Non-synchronized data signals do not disturb the black level of the internal signals.

Blanking of RGB and data signals

Both the RGB and data signals can be blanked via the sandcastle input (pin 7). A slicing level of 1.5 V is used for this blanking function, so that the wide part of the sandcastle pulse is separated from the remainder of the pulse. During blanking a level of +1 V is available at the output. To prevent parasitic oscillations on the third overtone of the crystal the optimum tuning capacitance should be 10 pF.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 1)	–	13.2	V
P_{tot}	total power dissipation	–	1700	mW
T_{amb}	operating ambient temperature	–25	+70	°C
T_{stg}	storage temperature	–25	+150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	40 K/W

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; all voltages are referenced to pin 27; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage		10.8	12.0	13.2	V
I_P	supply current		–	90	120	mA
P_{tot}	total power dissipation		–	1.1	1.6	W
Luminance input (pin 8)						
$V_{8(p-p)}$	input voltage (peak-to-peak value)	note 1	–	0.45	0.63	V
V_8	input voltage level before clipping occurs in the input stage		–	–	1.4	V
I_8	input current		–	0.1	1	μA
	contrast control range	see Fig.3	–11.5	–	+5	dB
I_6	input current contrast control		–	–	15	μA
Chrominance amplifier						
$V_{4(p-p)}$	input signal amplitude (peak-to-peak value)	note 2	40	390	1100	mV
$\|Z_4\|$	input impedance		–	10	–	kΩ
C_4	input capacitance		–	–	6.5	pF
	ACC control range		30	–	–	dB
ΔV	change of the burst signal at the output control range	100 mV to 1 V (p-p)	–	–	1	dB
G	amplification at nominal saturation (pin 4 to pin 28)	note 3	34	–	–	dB
	chrominance to burst ratio at nominal saturation		–	7	–	dB
$V_{28(p-p)}$	maximum output voltage range (peak-to-peak value)	R_L = 2 kΩ	4	5	–	V
d	distortion of chrominance amplifier at 2 V (p-p) output signal up to an input signal of 1 V (p-p)		–	–	5	%
α_{28-4}	frequency response between 0 and 5 MHz		–	–	–2	dB
	saturation control range	see Fig.4	50	–	–	dB
I_5	input current saturation control		–	–	20	μA
	cross-coupling between luminance and chrominance amplifier	note 4	–	–	–46	dB
S/N	signal-to-noise ratio at nominal input signal	note 5	56	–	–	dB
Δφ	phase shift burst with respect to chrominance at nominal saturation		–	–	±5	deg
$\|Z_{28}\|$	output impedance of chrominance amplifier		–	10	–	Ω

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{28}	output current		–	–	15	mA
Reference part						
Δf	phase-locked loop catching range	note 6	500	–	–	Hz
Δφ	phase shift for 400 Hz deviation of the oscillator frequency	note 6	–	–	5	deg
TC_{osc}	oscillator temperature coefficient with respect to oscillator frequency	note 6	–	–2	–3	Hz/K
Δf_{osc}	frequency deviation when supply voltage increases from 10 to 13.2 V	note 6	–	40	100	Hz
R_{26}	input resistance		280	400	520	Ω
C_{26}	input capacitance		–	–	10	pF
ACC generation (pin 2; note)7						
V_2	control voltage at nominal input signal		–	4.5	–	V
V_2	control voltage without chrominance input		–	2	–	V
ΔV_2	colour-on/off voltage		175	300	425	mV
V_2	colour-on voltage		3.1	3.5	3.9	V
ΔV_2	colour-on identification voltage		1.2	1.5	1.8	V
	change in burst amplitude with temperature		–	0.1	0.25	%/K
V_3	voltage at pin 3 at nominal input signal		–	4.7	–	V
Demodulator part						
$V_{23(p-p)}$	amplitude of burst signal (peak-to-peak value) between pins 23 and 27	note 8	45	63	81	mV
$\|Z_{22, 23}\|$	input impedance between pins 22 or 23 and 27		0.7	1.0	1.3	kΩ
RATIO OF DEMODULATED SIGNALS FOR EQUIVALENT INPUT SIGNALS AT PINS 22 AND 23						
$\frac{V_{17}}{V_{13}}$	(B–Y)/(R–Y)		–	1.78 ± 10%	–	
$\frac{V_{15}}{V_{13}}$	(G–Y)/(R–Y)	no (B–Y) signal	–	–0.51 ± 10%	–	
$\frac{V_{15}}{V_{17}}$	(G–Y)/(B–Y)	no (R–Y) signal	–	–0.19 ± 25%	–	
α_{17}	frequency response between 0 and 1 MHz		–	–	–3	dB
α_{cr}	cross-talk between colour difference signals		40	–	–	dB
Δφ	phase difference between (R–Y) and (B–Y) reference signals		85	90	95	deg

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\Delta\varphi_{tot}$	total phase difference between chrominance input signals and demodulator output signals		–	–	8	deg
RGB matrix and amplifiers						
$V_{13, 15, 17(p-p)}$	output voltage (peak-to-peak value) at nominal luminance/contrast (black-to-white)	note 3	3.3	3.8	4.3	V
$V_{13(p-p)}$	output signal amplitude of the 'RED' channel (peak-to-peak value) at nominal contrast/saturation and no luminance signal to the input (R–Y signal)		–	3.7	–	V
$V_{13, 15, 17(m)}$	maximum peak-white level		9.4	10.0	10.6	V
$I_{13, 15, 17}$	available output current		10	–	–	mA
$\Delta V_{13, 15, 17}$	difference between black level and measuring level at the output for a brightness control voltage of 2 V	note 9	–	0	–	V
ΔV	difference in black level between the three channels for equal drive conditions for the three gains	note 10	–	–	100	mV
	control range of black-current stabilization at V_{black} = 3 V; V_{11} = 2 V		–	–	±2	V
ΔV	black level shift with picture content		–	–	40	mV
	brightness control voltage range	see Fig.5	–	–	–	V
I_{11}	brightness control input current		–	–	5	μA
	slope of brightness control curve		–	1.3	–	V/V
	tracking of contrast control between the three channels over a control range at 10 dB		–	–	0.5	dB
V_o	output voltage during test pulse after switch-on		6.5	7.3	–	V
$\frac{\Delta V}{\Delta T}$	variation of black level with temperature		–	0	–	mV/K
ΔV	variation of black level with contrast (+5 to –10 dB)	note 11	–	–	100	mV
	relative spread between the three output signals		–	–	10	%
ΔV	relative black level variation between the three channels during variation of contrast, brightness and supply voltage	note 11	–	0 ± 10%	20 ± 10%	mV
V_{blk}	blanking level at the RGB outputs		–	0.85	1.1	V
ΔV_{blk}	difference in blanking level of the three channels		–	0	10	mV
dV_{blk}	differential drift of the blanking levels	ΔT = 40 °C	–	0	10	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\frac{\Delta V_{bl}}{V_{bl}} \times \frac{V_{Pl}}{\Delta V_{Pl}}$	tracking of output black level with supply voltage		0.9	1.0	1.1	
S/N	signal-to-noise ratio of output signals	note 5	62	–	–	dB
$V_{R(p-p)}$	residual 4.4 MHz signal at RGB outputs (peak-to-peak value)		–	–	100	mV
$V_{R(p-p)}$	residual 8.8 MHz signal and higher harmonics at the RGB outputs (peak-to-peak value)		–	–	150	mV
$\|Z_o\|$	output impedance (pins 13, 15 and 17)		–	100	–	Ω
α_{tot}	frequency response of total luminance and RGB amplifier circuits for f = 0 MHz and 5 MHz		–	–1	–3	dB
I_o	current source of output stage		2	3	–	mA
ΔV	difference of black level at the three outputs at nominal brightness	note 11	–	–	10	mV
	tracking of brightness control		–	–	2	%
Data insertion						
$V_{12, 14, 16(p-p)}$	input signals (peak-to-peak value) for an RGB output voltage of 3.8 V (peak-to-peak) at nominal contrast	note 4	0.9	1.0	1.1	V
ΔV	difference between the black level of the RGB signals and the black level of the inserted signals at the outputs at nominal contrast	note 12	–	–	170	mV
t_r	output rise time		–	50	80	ns
t_d	difference delay for the three channels		–	0	40	ns
$I_{12, 14, 16}$	input current		–	–	10	μA
Data blanking						
V_9	input voltage for no data insertion		–	–	0.3	V
V_9	input voltage for data insertion		0.9	–	–	V
V_9	maximum input pulse voltage		–	–	3	V
t_d	delay of data blanking		–	–	20	ns
R_9	input resistance		7	10	13	kΩ
	suppression of the internal RGB signals when $V_9 > 0.9$ V		46	–	–	dB
	suppression of external RGB signals when $V_9 < 0.3$ V		46	–	–	dB
Sandcastle input (note 13)						
V_7	level at which the RGB blanking is activated		1.0	1.5	2.0	V
V_7	level at which the horizontal pulses are separated		3.0	3.5	4.0	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_7	level at which the burst gate and clamping pulse are separated		6.5	7.0	7.5	V
t_d	delay between black level clamping and burst gating pulse		–	0.6	–	μs
I_i	input current	V_i = 0 to 1 V	–	–	–1	mA
		V_i = 1 to 8 V	–	–	50	μA
		V_i = 8 to 12 V	–	–	2	mA
Black current stabilization						
V_{18}	DC bias voltage		3.5	5.0	7.0	V
ΔV	difference between input voltage for black current and leakage current		0.35	0.5	0.65	V
I_{18}	input current during black current		–	–	1	μA
I_{18}	input current during scan		–	–	10	mA
V_{18}	internal limiting at pin 18		8.5	9.0	9.5	V
V_{18}	switching threshold for black current control on		7.6	8.0	8.4	V
R_{18}	input resistance during scan		1.0	1.5	2.0	kΩ
$I_{10, 20, 21}$	DC input current during scan at pins 10, 20 and 21		–	–	30	nA
	maximum charge or discharge current during measuring time (pins 10, 20 and 21)		–	1	–	mA
	difference in drift of the blank level	note 11; ΔT = 40 °C		0	20	mV
NTSC						
$V_{24\text{-}25}$	level at which the PAL/NTSC switch is activated (pins 24 and 25)		–	8.8	9.2	V
$I_{24+25\ (AV)}$	average output current (pin 24 plus pin 25)	note 14	62	82.5	103	μA
HUE	hue control	see Fig.6	–	–	–	

Notes to the characteristics

1. Signal with the negative-going sync; amplitude includes sync pulse amplitude.
2. Indicated is a signal with 75% colour bar, so the chrominance-to-burst ratio is 2.2 : 1.
3. Nominal contrast is specified as the maximum contrast –5 dB and nominal saturation as maximum –6 dB. This figure is valid in the PAL-condition. In the NTSC-condition no output signal is available at pin 28.
4. Cross coupling is measured under the following condition: input signal nominal, contrast and saturation such that nominal output signals are obtained. The signals at the output at which no signal should be available must be compared with the nominal output signal at that output.
5. The signal-to-noise ratio is defined as peak-to-peak signal with respect to RMS noise.
6. All frequency variations are referenced to the 4.4 MHz carrier frequency. All oscillator specifications have been measured with the Philips crystal 4322 143 ... or 4322 144 ... series.
7. The change in burst with V_P is proportional.

8. These signal amplitudes are determined by the ACC circuit of the reference part.
9. This value depends on the gain setting of the RGB output amplifiers and the drift of the picture tube guns. Higher black level values are possible (up to 5 V) however, in that condition the amplitude of the available output signal is reduced.
10. The variation of the black-level during brightness control in the three different channels is directly dependent on the gain of each channel. Discolouration during adjustments of contrast and brightness does not occur because amplitude and the black-level change with brightness control are directly related.
11. With respect to the measuring pulse.
12. This difference occurs when the source impedance of the data signals is 150 Ω and the black level clamp pulse width is 4 μs (sandcastle pulse). For a lower impedance the difference will be lower.
13. For correct operating of the black level stabilization loop, the leading and trailing edges of the sandcastle pulse (measured between 1.5 V and 3.5 V) must be within 200 ns and 600 ns respectively.
14. The voltage at pins 24 and 25 can be changed by connecting the load resistors (20 kΩ, 1%, in this condition) to the slider bar of the hue control potentiometer (see Fig.6). When the transistor is switched on, the voltage at pins 24 and 25 is reduced below 9 V, and the circuit is switched to NTSC mode. The width of the burst gate is assumed to be 4 μs typical.

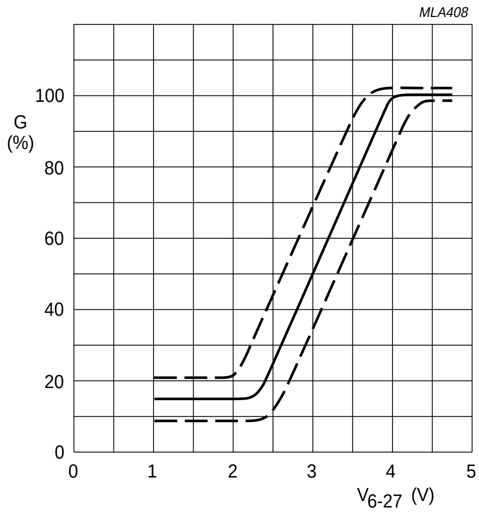


Fig.3 Contrast control voltage range.

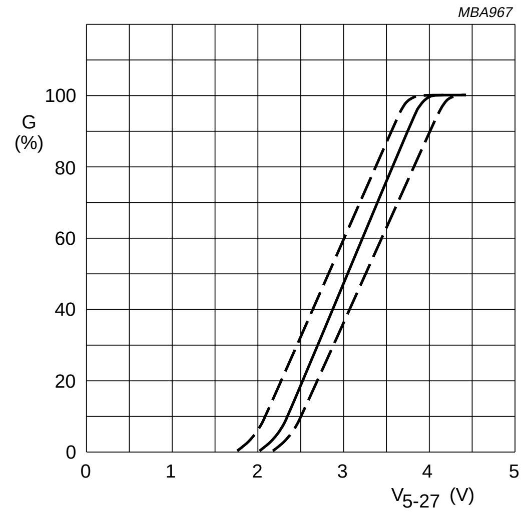


Fig.4 Saturation control voltage range.

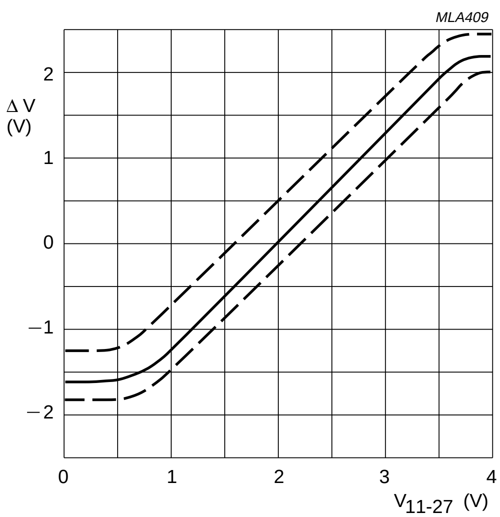


Fig.5 Difference between black level and measuring level at the RGB outputs (ΔV) as a function of the brightness control input voltage (V_{11}).

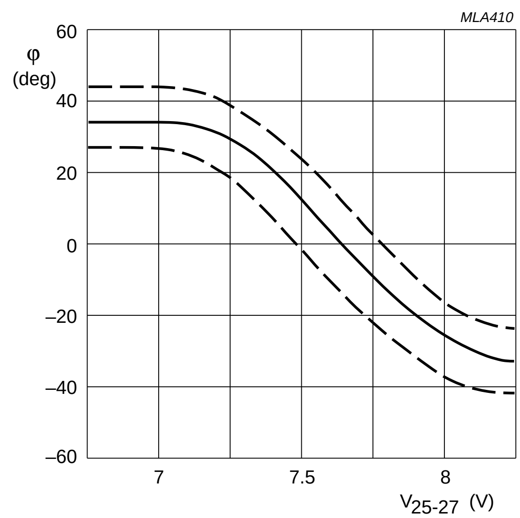


Fig.6 Hue control voltage range.

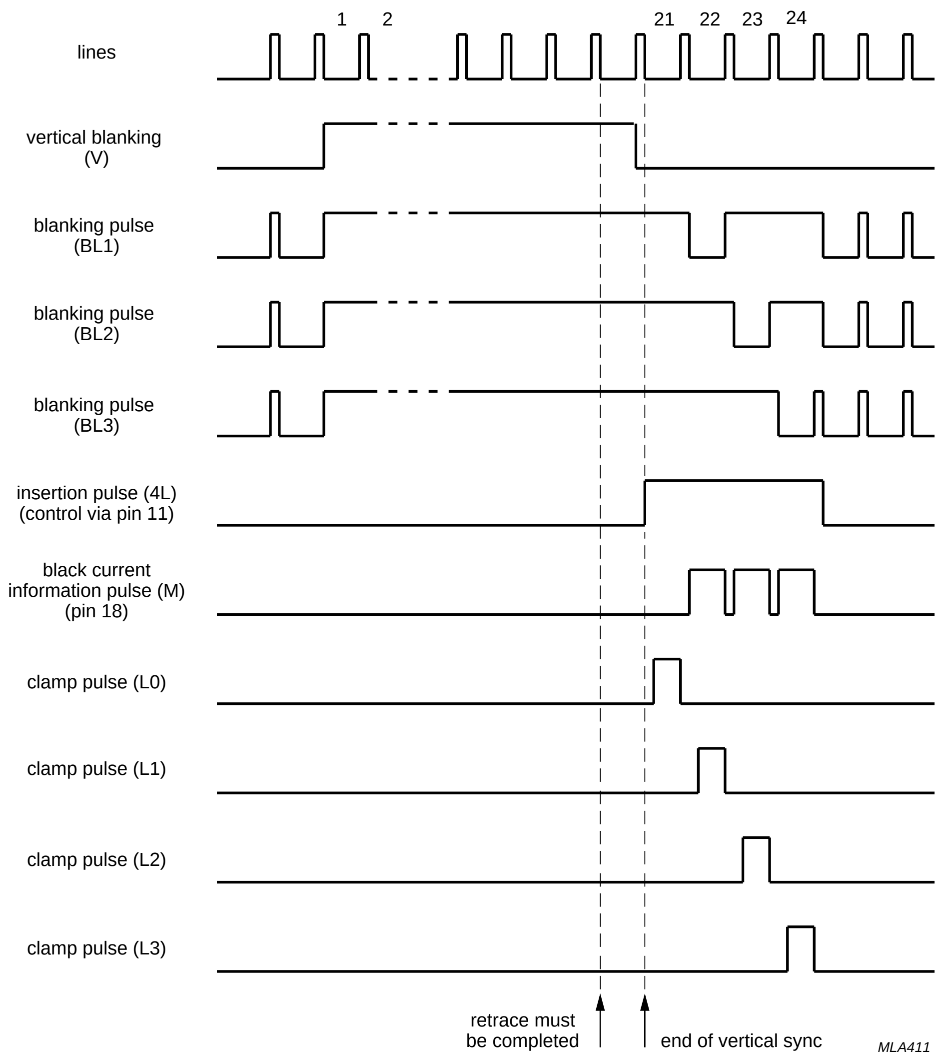


Fig.7 Timing diagram for black-current stabilization.

APPLICATION INFORMATION

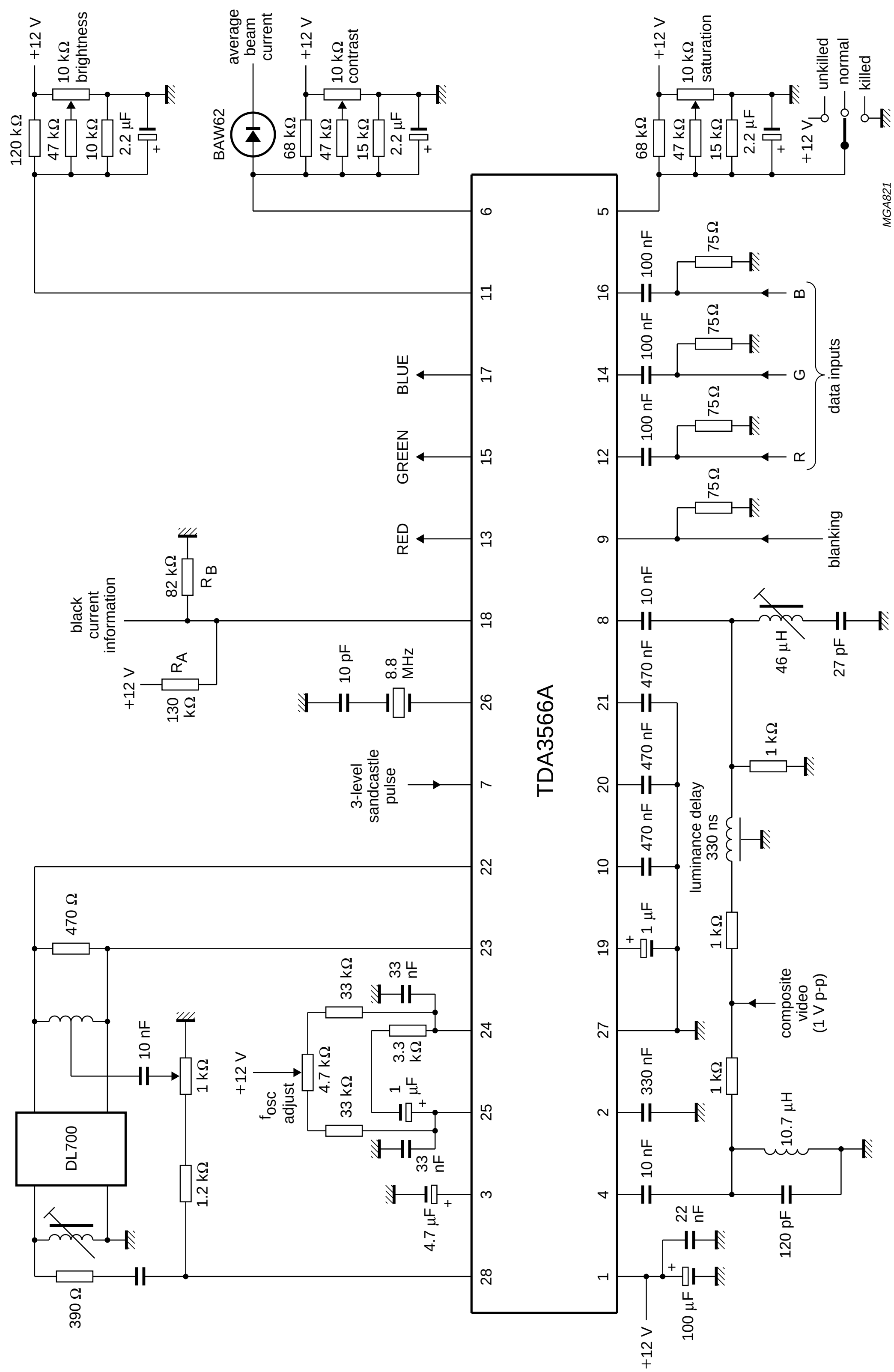


Fig.8 Application diagram showing the TDA3566A for a PAL decoder.

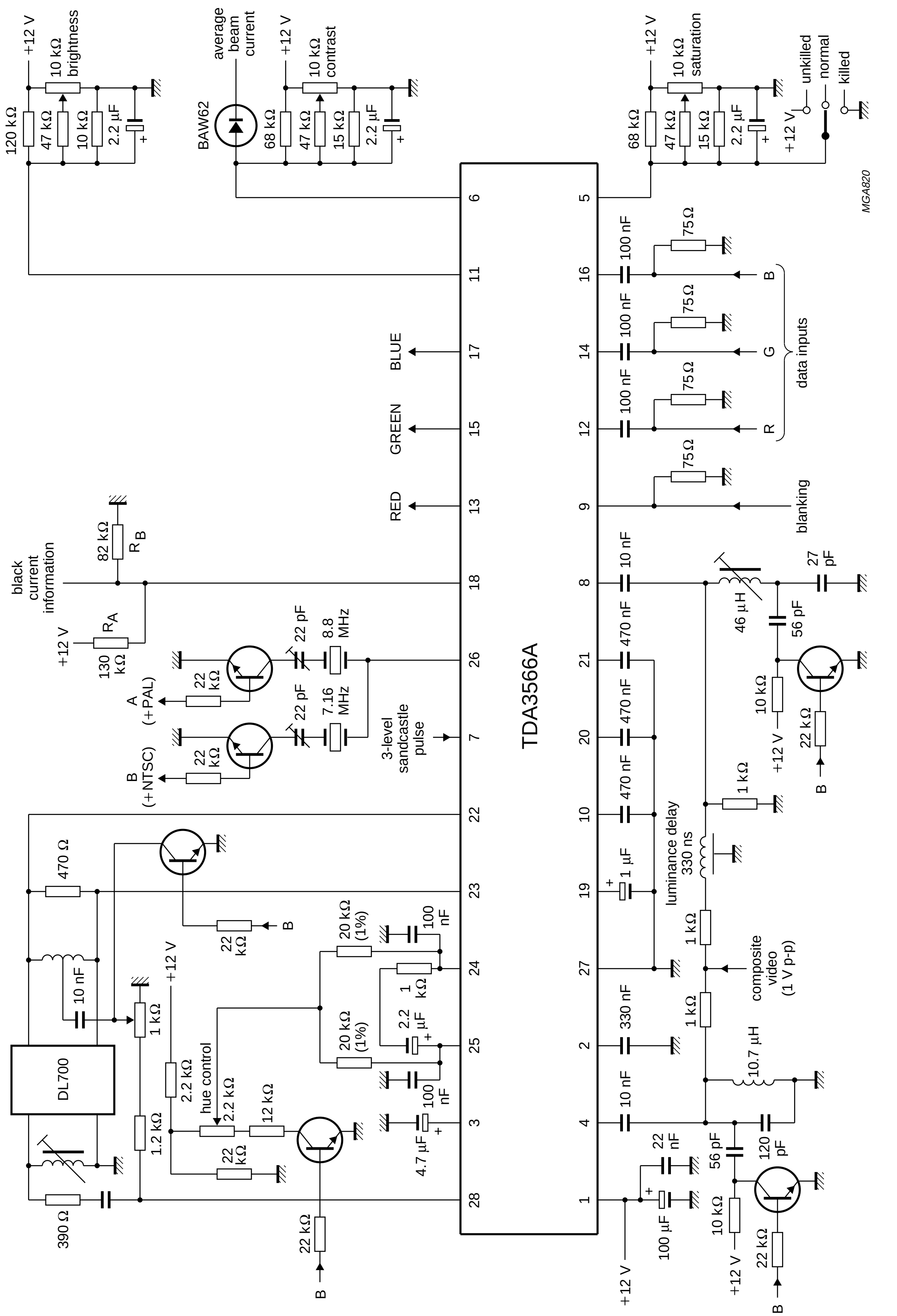


Fig.9 Application diagram showing the TDA3566A for a PAL/NTSC decoder.

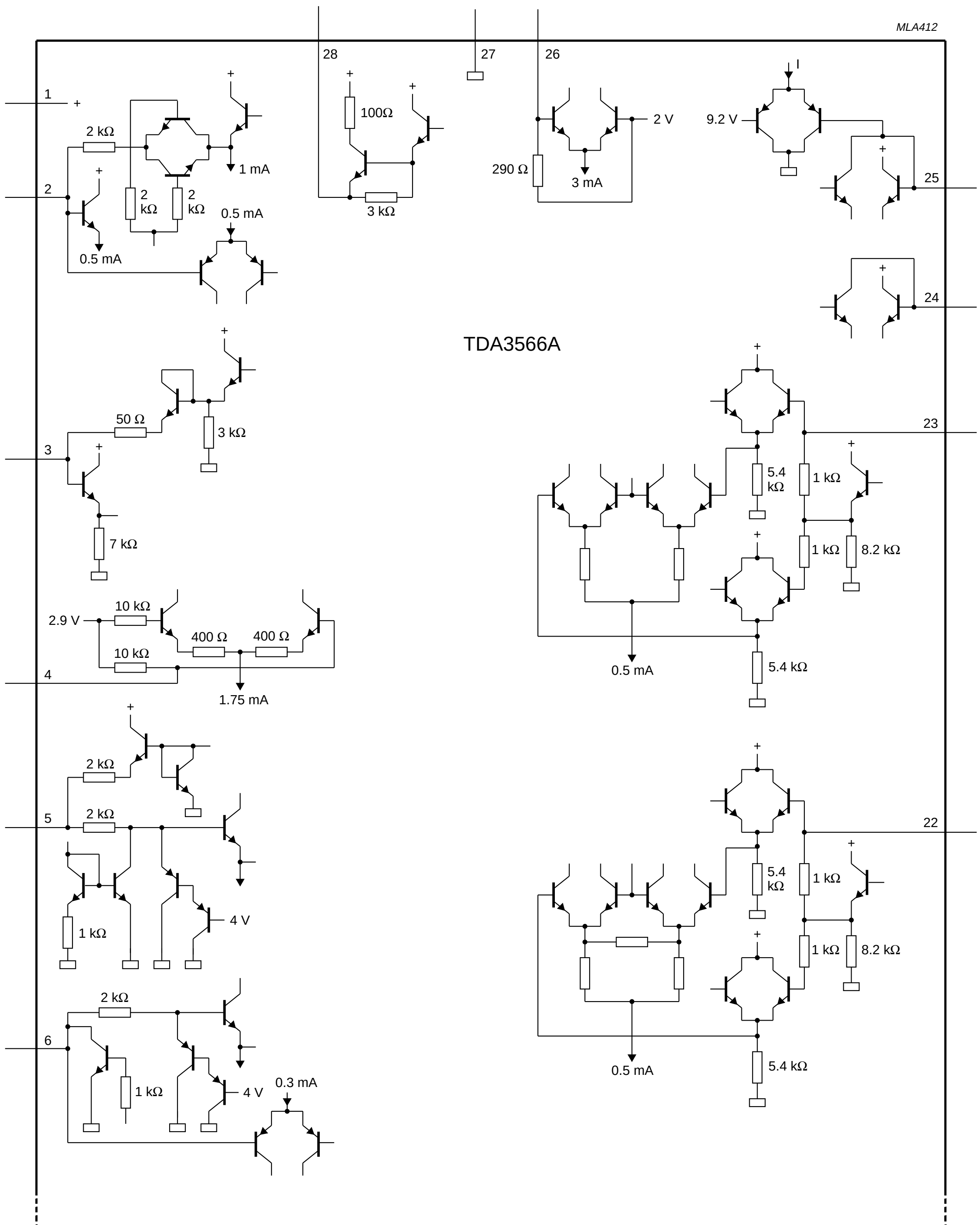


Fig.10 Internal pin circuitry (first part).

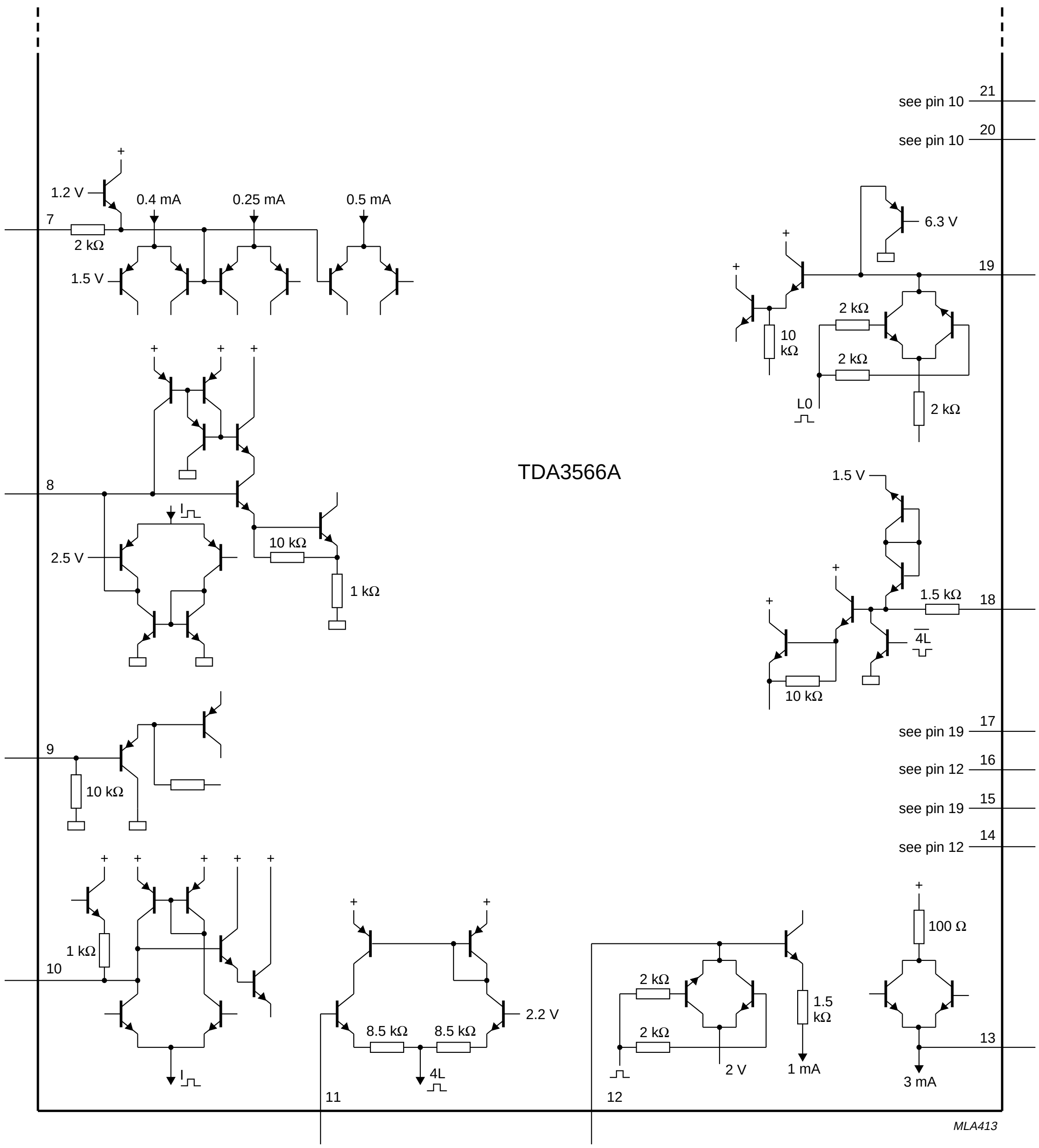
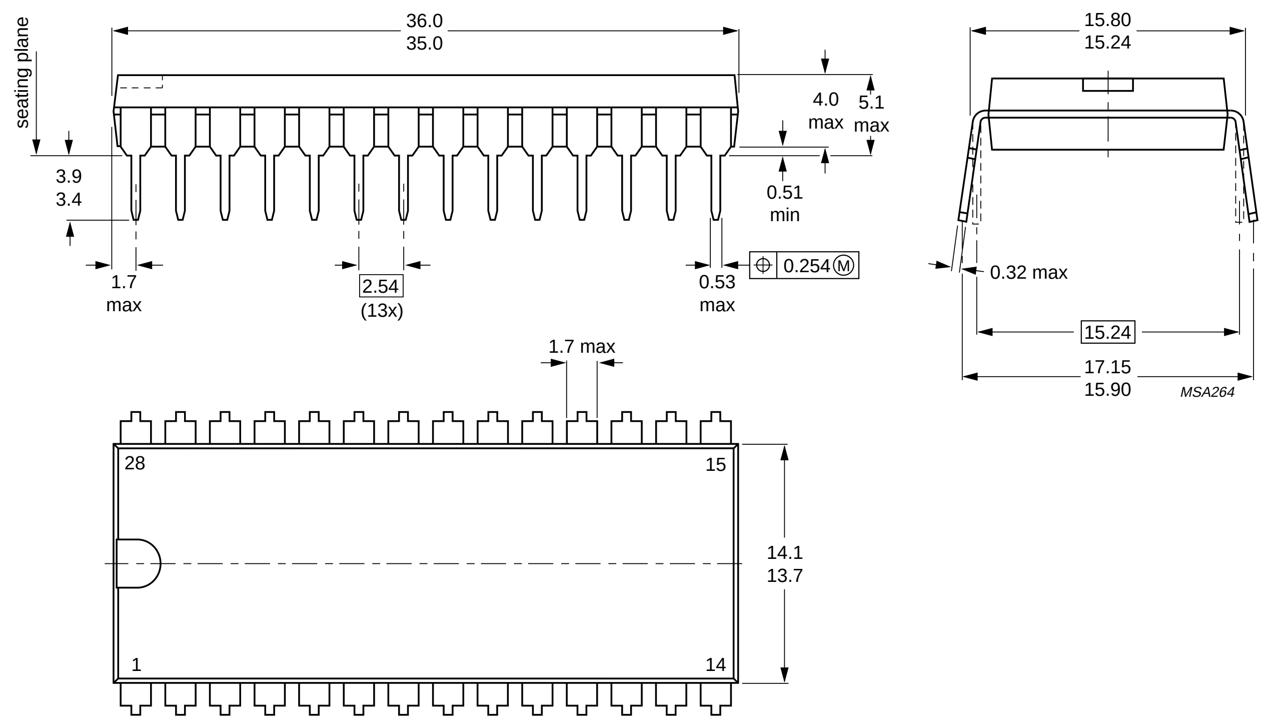


Fig.11 Internal pin circuitry (second part).

PACKAGE OUTLINE



Dimensions in mm.

Fig.12 28-lead dual in-line; plastic with internal heat spreader (SOT117).

SOLDERING

Plastic dual in-line packages

BY DIP OR WAVE

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 s. The total contact time of successive solder waves must not exceed 5 s.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply the soldering iron below the seating plane (or not more than 2 mm above it. If its temperature is below 300 °C, it must not be in contact for more than 10 s; if between 300 and 400 °C, for not more than 5 s.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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NOTES

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